CLAIMS

1. A decoder for decoding encoded data, the decoder comprising:

a processor having an input which receives probability estimates for a block of symbols, and which is arranged to calculates probability estimates for said symbols in a next iterative state;

normalising means which normalises said next states estimates;

a switch that receives both said normalised and said unnormalised next state estimates, the output of the switch being coupled to the input of the processor;

wherein the switch is arranged to switch between the normalised and unnormalised next state estimates depending on the iterative state.

2. A decoder according to claim 1 wherein said decoder comprises a MAP algorithm wherein the probability estimates are α and β values.

3. A decoder according to claim 1 wherein said decoder has eight iterative states for each received symbol block.

4. A decoder according to claim 1 wherein the ratio between said unnormalised and said normalised next state estimates is 7:1.

5. A decoder according to claim 1 wherein said switch is a multiplexer.

6. A decoder according to claim 1 further comprising pipeline registers between said processor and said normalising function.

7. A turbo decoder comprising a decoder according to claim 1.

8. A decoder for decoding encoded data, the decoder comprising:

a processor having an input which receives probability estimates for a block of symbols, and which is arranged to calculate probability estimates for said symbols in a next iterative state;

normalising means coupled to the processor which normalises said next states estimates;

wherein the decoder further comprises pipelining means between the processor and the normalising means for providing non-normalised next state estimates.

9. A decoder as claimed in claim 8 further comprising switching means that receives both said normalised and said unnormalised next state estimates, the output of the switch being coupled to the input of the processor;

wherein the switch is arranged to switch between the normalised and unnormalised next state estimates depending on the iterative state.

10. A decoder according to claim 8 wherein said pipelining means is a pipeline register coupled between outputs of said processor and inputs of said normalising means.